

Answers to Question form the March 25-26, 1999 ROD Review

December 17, 1999

Wisconsin

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Answers to Question form the March 25-26, 1999 ROD Review

Question:

While the FPGA development is quite advanced, the development of the DSP part seems, by comparison, at a very early stage. There are many non-trivial engineering details to work out in order to integrate the DSPs into the ROD properly. In this area, the expertise of UCI is critically needed.

Response:

The DSP component and back end processing tasks are better understood at this time. Test have been made that determined that a floating point DSP is better matched to the monitoring and calibration tasks. The architecture for the DSPs is better understood. The loss of UCI to the DSP effort has been addressed by John Joseph addressing the hardware aspects of the DSP and having Eli Rosenberg and Tom Meyer join in the effort to program applications for calibration and monitoring. A DSP test card has been sent to them. It is currently being made operational. They will also bring one student into this effort.

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Question:

As for technical risk of the FPGA solution, the utilization of the particular FPGA proposed for the Decoder appears to be quite tight. We recommend that the design move now to the larger FPGA in order to provide more flexibility to cope with unforeseen problems.

Response:

The FPGAs have been changed from Orca to XILINX. This has resulted in the decoder FIFOs being included in the part. The current utilization is less than 64%.

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Question:

The committee feels that it is important that the ROD designers carefully consider the current and possible future need to access the various pieces of information available in the ROD, e.g. S-Link status, buffer occupancy information, front end status, etc. As much of this information as possible needs to be made available to the ROD controller. .

Response:

The monitoring of status has been included in the design. This information is available to the ROD controller.

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Question:

Connections should be made between unused pins on the FPGAs to mitigate the risk of unforeseen requirements. These provisions are important both to handle unforeseen circumstances and to ease the debugging of the board.

Response:

Unused connection have been made between FPGAs.

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Question:

While the committee feels strongly that the software should be engineered as fully and as carefully as the hardware, given its importance to the overall ROD design. **By software, we mean both the DSP program running in the ROD as well as the interfaces and low level primitives used to access the ROD from the ROD Crate Controller.**

Response:

This software needs to be carefully designed and implemented and needs to be reviewed at each phase. The software needs to be managed and versioned not only for released code, but also during development. Documentation must also be maintained throughout the process. This will help complete the ROD on schedule and will ease maintenance.

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Response:

The software has been organized such that the initial software will be supplied by the ROD group. This will include maintenance/debugging, low level primitives, initial histogramming/event trapping and error detection software. It is strongly believed that control of the final software must be in the hands of the user community. If the ROD group tried to provide all of the DSP and primitive software, It would become untenable in the long term as request for changes would be funneled through one group with the inevitable needs to understand the requests and the potential for a single point failure. Two centers for the long term software are planned to be establish one in the US (pixel specific DAQ EliRosenberg, etc.) and one in the UK (SCT specific DAQ John Hill, etc.). Lukas is currently designing the high level architecture for the test stand software in consultation with John Hill. Tom Meyer is currently at LBNL with the pixel DAQ perspective in mind. This close association with the user communities will do much to allow for the incorporation of the ROD group software in the SCT DAQ and pixel DAQ with minimal problems. It will also be very useful to have their input into the design of the software being done by the ROD group.

The software performed by the ROD group will be designed carefully with frequent reviews by the user community. Version control will be done at all stages with accompanied documentation of the code and architecture.

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Question:

Of greater concern to the committee was the significant time lost from the schedule in coming to conclusion for the choice of architecture. There still exists sufficient time to deliver the first articles of the production ROD, for the important SCT production barrel tests by September 2001 with prototypes made available to SCT module test by February 2000. The ROD engineering team will need to work closely with the Atlas SCT, Pixel, and DAQ communities to finalize the requirements for the ROD now and should not view ROD99 or the prototype as a means to discover new architectural requirements.

Response:

The preprototype ROB and the prototype ROD have been merged to maximize the probability of producing the ROD on schedule. The current schedule calls for the ROD to be available to the user community by April of 2000. This is the same time frame as the TIM (Timing Interface Module) and BOC (Back Of Crate (optical interface)) cards. These two cards are required to operate the ROD in the data taking mode. The schedule is tight but doable for all three cards and will allow for the essential user evaluation of the ROD system in 2000. The production ROD for 2001 should be no problem.

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Question:

However, the review committee suggests that the manpower estimate needed for completion of the work is understated and should be reviewed again..

Response:

	ROD	SCT DAQ	Pixel DAQ
Physicist	1	0.25	0.65
EE	3.45	0	0

EE R. Jared (.25), M. Nagel (1.0), J. Joseph (1.0), K. Dao (0.2), L. Tomasek (SW) (1)
Phy. D. Fashing (1.0), E. Rosenberg (0.25), Tom Meyer (0.4), J. Hill (0.25)

The manpower is consistent with the cost to complete and should be adequate.